

REMARKS

The applicant notes with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicant acknowledges and appreciates receiving an initialed copy of the form PTO-1449 that was filed on November 4, 2003.

Claims 1 and 3 – 28 are pending. Claim 2 has been canceled. Claims 6 – 25 have been withdrawn. The applicant respectfully requests reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1, 2, 4 and 5 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent No. 6,504,227, Matsuo et al. (“Matsuo”) in view of U.S. Patent No. 4,571,819, Rogers et al. (“Rogers”). Claim 3 was rejected under 35 USC 103(a) as being unpatentable over Matsuo in view of Rogers, further in view of U.S. Patent No. 6,245,600, Geissler et al. (“Geissler”). The rejection is respectfully traversed for reasons including the following, which are provided by way of example.

As described in the application, one or more aspects recognize the problem of thermal expansion (e.g., specification page 10, lines 18 - 24). Independent claim 1 recites in combination, for example, “a thermal-oxide layer of 10 μm or more in thickness is formed in a region where the first device components are to be disposed, and a groove packed with a polycrystalline semiconductor is formed at an inward position from the peripheral edge of the thermal-oxide layer and along the same peripheral edge, said thermal-oxide layer having been made into an oxide by thermally oxidizing a base material semiconductor.” Independent claim 26 further recites, in combination, for example, the groove packed with a polycrystalline semiconductor

“having a depth larger than the thickness of the thermal-oxide layer.” The semiconductor substrate can be prevented from warping and causing crystal defects, where the groove is packed with crystalline semiconductor, the thermal stress can be absorbed up to the lower part of the thick thermal-oxide layer region in the step of forming device components on the semiconductor substrate. (See, e.g., page 11, lines 2 – 13.)

To properly reject a claimed invention, the examiner must establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness with respect to a claimed invention, all the claim limitations must be taught or suggested by the prior art reference (or references when combined). *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Furthermore, the teaching or suggestion to make the claimed combination and a reasonable expectation of success must both be found in the prior art and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991).

The examiner bears the burden of establishing this *prima facie* case. *In re Deuel*, 34 U.S.P.Q.2d 1210, 1214 (Fed. Cir. 1995). The applicant for patent may then attack the *prima facie* case as improperly made out, or present objective evidence tending to support a conclusion of nonobviousness. *In re Fritch*, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992).

Where, as here, the examiner fails to establish a *prima facie* case of obviousness, the applicant has no burden to rebut the rejection of obviousness with evidence. *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993). If the examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of patent. *In re Oetiker*, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992).

The applicants provide herein a selection of some examples of limitations in the claims which are neither taught nor suggested by Matsuo. The final Office Action admits that Matsuo fails to teach “the oxide layer being a thermal-oxide.” Also, the office action admits that Matsuo fails to teach that “a groove packed with a polycrystalline semiconductor is formed at an inward position from the peripheral edge of the thermal-oxide layer and along the same peripheral edge.” (Office Action pages 2 - 3). Recognizing that Matsuo fails to teach and/or suggest the invention as claimed, Rogers is cited to remedy the deficiencies.

Nevertheless, Rogers fails to remedy such deficiencies. For example, the oxide taught by Rogers is an oxide formed by CVD. Accordingly, Rogers fails to teach or suggest an oxide formed by thermal oxidation. Moreover, Rogers is not concerned with the problem of volume expansion at the time of thermal oxidation.

Hence, Matsuo and Rogers, alone or in combination, fail to teach or suggest the combination of features recited in independent claim 1, when considered as a whole.

Furthermore, Matsuo and/or Rogers are fundamentally different from the claimed invention. Specifically, Matsuo presupposes a process in which a groove is formed in a substrate on which an active element has been formed (i.e., after an active element has been formed on a substrate) and then the groove is packed with an oxide. In Matsuo, after the groove is packed with an oxide, there is no thermal heat treatment because of the thermal stress that may be applied to the semiconductor substrate which may warp or cause crystal defects. In Rogers as all, the polycrystalline semiconductor with which the groove is packed is only utilized for the function of the etch-stop during the planarization process (e.g., col. 5, beginning at line 33); any function for relieving the stress produced during heat treatment is not considered at all. To the contrary, Rogers provides for forming an additional oxide layer for the purpose of stress relief

(e.g., col. 5, lines 30 – 33). The Office Action cites the Matsuo as disclosing the thermal-oxide limitation, however, both Matsuo and Rogers are clearly deficient considering the invention as claimed as a whole. Consequently, the proposed combination fails to teach or suggest the claimed invention.

With respect to the rejected dependent claims, applicant respectfully submits that these claims are allowable not only by virtue of their dependency from independent claim 1, but also because of additional features they recite in combination.

New claims 26 – 28 have been added to further define the invention, and are believed to be patentable for reasons including these set out above. New claim 26 corresponds to claim 2 written in independent form (incorporating claim 1 as amended); accordingly, claim 2 has been canceled. Support for the amendment to claim 1 is located in the specification, for example, page 6, line 22 – page 7, line 1; page 12, lines 13 - 18. Support for new claims 27 – 28 is located in the specification, for example on page 34, lines 5 – 16.

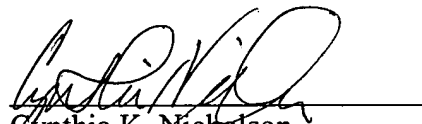
Applicant respectfully submits that, as described above, the cited prior art does not show or suggest the combination of features recited in the claims. Applicant does not concede that the cited prior art shows any element recited in the claims. However, applicant has provided specific examples of elements in the claims that are clearly not present in the cited prior art.

Applicant strongly emphasizes that one reviewing the prosecution history should not interpret any of the examples applicant has described herein in connection with distinguishing over the prior art as limiting to those specific features in isolation. Rather, for the sake of simplicity, applicant has provided examples of why the claims described above are distinguishable over the cited prior art.

In view of the foregoing, the applicant respectfully submits that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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